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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 08/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/773,850	EICHLER ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20040112*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 4, 6, 7, 10, 12, 13, 16, 18, 22, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 5,819,053 to Goodrum et al. ("Goodrum").

3. In reference to Claim 1, Goodrum teaches a method executed internal to a computing device for identifying an available peripheral component interconnect (PCI) slot in the computing device, comprising: identifying a plurality of PCI slots in the computing device (See Column 95 Lines 16-33); identifying at least one PCI device coupled to a PCI bus, the PCI bus coupled to the PCI slot (See Column 95 Lines 29-31); and identifying, without requiring physical inspection of the PCI slots, an unoccupied PCI slot, an unoccupied PCI slot comprising an identified PCI slot that is not coupled to an identified PCI device (See Column 95 Lines 53-65).

4. In reference to Claim 4, Goodrum teaches the limitations as applied to Claim 1 above. Goodrum further teaches identifying a bus number and a device number for each PCI device coupled to the PCI bus (See Column 95 Lines 35-49).

5. In reference to Claim 6, Goodrum teaches the limitations as applied to Claim 1 above. Goodrum further teaches reserving a bus number for each empty slot, and thus identifies how many identified PCI slots are unoccupied (See Column 95 Line 66 – Column 96 Line 11).

6. In reference to Claim 7, Goodrum teaches a system for identifying an available peripheral component interconnect (PCI) slot in a computing device by executing an application internal to the computing device, comprising: at least one computer readable medium (See Figure 1 Number 23 and Column 95 Lines 31-33); and software encoded on the at least one computer readable medium (See Column 95 Lines 26-33) and operable when executed by a processor to: identify a plurality of PCI slots in the computing device (See Column 95 Lines 16-33), identify at least one PCI device coupled to a PCI bus, the PCI bus coupled to the PCI slot (See Column 95 Lines 29-31); and identify, without requiring physical inspection of the PCI slots, an unoccupied PCI slot, an unoccupied PCI slot comprising an identified PCI slot that is not coupled to an identified PCI device (See Column 95 Lines 53-65).

7. In reference to Claim 10, Goodrum teaches the limitations as applied to Claim 7 above. Goodrum further teaches identifying a bus number and a device number for each PCI device coupled to the PCI bus (See Column 95 Lines 35-49).

8. In reference to Claim 12, Goodrum teaches the limitations as applied to Claim 7 above. Goodrum further teaches reserving a bus number for each empty slot, and thus identifies how many identified PCI slots are unoccupied (See Column 95 Line 66 – Column 96 Line 11).

9. In reference to Claim 13, Goodrum teaches a system for identifying an available peripheral component interconnect (PCI) slot in a computing device by executing a process internal to the computing device, the system comprising: a memory operable to store information identifying a plurality of PCI slots in the computing device (See Figure 1 Number 20 and Column 95 Lines 16-25); and a processor coupled to the memory (See Figure 1 Number 14) and operable to: identify at least one PCI device coupled to a PCI bus, the PCI bus coupled to the PCI slot (See Column 95 Lines 29-31); and identify, without requiring physical inspection of the PCI slots, an unoccupied PCI slot, an unoccupied PCI slot comprising an identified PCI slot that is not coupled to an identified PCI device (See Column 95 Lines 53-65).

10. In reference to Claim 16, Goodrum teaches the limitations as applied to Claim 13 above. Goodrum further teaches identifying a bus number and a device number for

each PCI device coupled to the PCI bus using a bus controller (See Column 95 Lines 35-49).

11. In reference to Claim 18, Goodrum teaches the limitations as applied to Claim 13 above. Goodrum further teaches reserving a bus number for each empty slot, and thus identifies how many identified PCI slots are unoccupied (See Column 95 Line 66 – Column 96 Line 11).

12. In reference to Claim 22, Goodrum teaches the limitations as applied to Claim 1 above. Goodrum further teaches creating a table, which is equivalent to generating a list, with information about the identified PCI slots associated with a computing device (See Column 95 Lines 16-25).

13. In reference to Claim 24, Goodrum teaches the limitations as applied to Claim 7 above. Goodrum further teaches creating a table, which is equivalent to generating a list, with information about the identified PCI slots associated with a computing device (See Column 95 Lines 16-25).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 2, 5, 8, 11, 14, 17, 23, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goodrum as applied to Claims 1, 7, and 13 above, and further in view of US Patent Number 6,397,268 to Cepulis ("Cepulis").

16. In reference to Claim 2, Goodrum teaches the limitations as applied to Claim 1 above. Goodrum does not teach that identifying a plurality of PCI slots in the computing device comprises identifying a bus number and a device number for the plurality of PCI slots using a PCI Interrupt Request (IRQ) routing table. Cepulis teaches the use of a PCI IRQ routing table to track PCI bus, device, and slot numbers for each PCI device slot (See Column 6 Lines 3-7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Goodrum with the PCI IRQ routing table use of Cepulis, resulting in the invention of Claim 2, in order to provide a computing device that uses the most accurate copy of the bus, device, and slot numbers, since the table was loaded at startup and thus will reflect the most up to date configuration information of the system (See Column 6 Lines 11-25 of Cepulis).

17. In reference to Claim 5, Goodrum teaches the limitations as applied to Claim 1 above. Goodrum does not teach that identifying an unoccupied PCI slot comprises

comparing a bus number and a device number of at least one of the identified PCI slots to a bus number and a device number of at least one of the identified PCI devices. Cepulis teaches comparing a PCI IRQ routing table for each PCI device slot (See Column 6 Lines 3-5) with an NVRAM data structure storing information about each PCI device in the computer system (See Column 5 Lines 54-61 and Column 6 Lines 26-28).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Goodrum with the PCI IRQ routing table use and comparison of Cepulis, resulting in the invention of Claim 5, in order to provide a computing device that uses the most accurate copy of the bus, device, and slot numbers, since the table was loaded at startup and thus will reflect the most up to date configuration information of the system, as well as to allow configuration of the PCI devices at startup if their bus numbers have changed since the last time the information about each device was stored (See Column 6 Lines 11-25 of Cepulis).

18. In reference to Claim 8, Goodrum teaches the limitations as applied to Claim 7 above. Goodrum does not teach that the software is operable to identify a plurality of PCI slots in the computing device comprises identifying a bus number and a device number for the plurality of PCI slots using a PCI Interrupt Request (IRQ) routing table. Cepulis teaches the use of a PCI IRQ routing table to track PCI bus, device, and slot numbers for each PCI device slot (See Column 6 Lines 3-7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Goodrum with the PCI IRQ routing table

use of Cepulis, resulting in the invention of Claim 8, in order to provide a computing device that uses the most accurate copy of the bus, device, and slot numbers, since the table was loaded at startup and thus will reflect the most up to date configuration information of the system (See Column 6 Lines 11-25 of Cepulis).

19. In reference to Claim 11, Goodrum teaches the limitations as applied to Claim 7 above. Goodrum does not teach that the software is operable to identify an unoccupied PCI slot comprises comparing a bus number and a device number of at least one of the identified PCI slots to a bus number and a device number of at least one of the identified PCI devices. Cepulis teaches comparing a PCI IRQ routing table for each PCI device slot (See Column 6 Lines 3-5) with an NVRAM data structure storing information about each PCI device in the computer system (See Column 5 Lines 54-61 and Column 6 Lines 26-28).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Goodrum with the PCI IRQ routing table use and comparison of Cepulis, resulting in the invention of Claim 11, in order to provide a computing device that uses the most accurate copy of the bus, device, and slot numbers, since the table was loaded at startup and thus will reflect the most up to date configuration information of the system, as well as to allow configuration of the PCI devices at startup if their bus numbers have changed since the last time the information about each device was stored (See Column 6 Lines 11-25 of Cepulis).

20. In reference to Claim 14, Goodrum teaches the limitations as applied to Claim 13 above. Goodrum does not teach that the processor is operable to generate the information identifying a plurality of PCI slots in the computing device comprises identifying a bus number and a device number for the plurality of PCI slots using a PCI Interrupt Request (IRQ) routing table. Cepulis teaches the use of a PCI IRQ routing table to track PCI bus, device, and slot numbers for each PCI device slot (See Column 6 Lines 3-7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Goodrum with the PCI IRQ routing table use of Cepulis, resulting in the invention of Claim 14, in order to provide a computing device that uses the most accurate copy of the bus, device, and slot numbers, since the table was loaded at startup and thus will reflect the most up to date configuration information of the system (See Column 6 Lines 11-25 of Cepulis).

21. In reference to Claim 17, Goodrum teaches the limitations as applied to Claim 13 above. Goodrum does not teach that the processor is operable to identify an unoccupied PCI slot comprises comparing a bus number and a device number of at least one of the identified PCI slots to a bus number and a device number of at least one of the identified PCI devices. Cepulis teaches comparing a PCI IRQ routing table for each PCI device slot (See Column 6 Lines 3-5) with an NVRAM data structure storing information about each PCI device in the computer system (See Column 5 Lines 54-61 and Column 6 Lines 26-28).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Goodrum with the PCI IRQ routing table use and comparison of Cepulis, resulting in the invention of Claim 17, in order to provide a computing device that uses the most accurate copy of the bus, device, and slot numbers, since the table was loaded at startup and thus will reflect the most up to date configuration information of the system, as well as to allow configuration of the PCI devices at startup if their bus numbers have changed since the last time the information about each device was stored (See Column 6 Lines 11-25 of Cepulis).

22. In reference to Claim 23, Goodrum teaches the limitations as applied to Claim 1 above. Goodrum does not teach that identifying at least one PCI device coupled to a PCI bus comprises generating a list of one or more PCI devices coupled to the PCI bus. Cepulis teaches generating an NVRAM data structure, which is equivalent to a list, that stores the information about each PCI device in the computer system (See Column 5 Lines 54-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Goodrum with the NVRAM list of PCI devices coupled to the PCI bus of Cepulis, resulting in the invention of Claim 23, in order to provide a means for storing the information regarding the presence of a device (See Column 5 Lines 38-42 of Cepulis) and to provide the information to the computer system faster upon startup (See Column 5 Lines 26-38 of Cepulis).

23. In reference to Claim 25, Goodrum teaches the limitations as applied to Claim 7 above. Goodrum does not teach that the software is operable to generate a list of one or more PCI devices coupled to the PCI bus to identify at least one PCI device coupled to a PCI bus. Cepulis teaches generating an NVRAM data structure, which is equivalent to a list, that stores the information about each PCI device in the computer system (See Column 5 Lines 54-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Goodrum with the NVRAM list of PCI devices coupled to the PCI bus of Cepulis, resulting in the invention of Claim 25, in order to provide a means for storing the information regarding the presence of a device (See Column 5 Lines 38-42 of Cepulis) and to provide the information to the computer system faster upon startup (See Column 5 Lines 26-38 of Cepulis).

24. Claims 3, 9, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goodrum and Cepulis as applied to Claims 2, 8, and 14 above, and further in view of the "PCI IRQ routing table Specification" from Microsoft Corporation ("Microsoft").

25. In reference to Claim 3, Goodrum and Cepulis teach the limitations as applied to Claim 2 above. Goodrum and Cepulis do not teach locating the routing table in a read-only memory in the computing device. Microsoft teaches locating the routing table in a ROM array (See Page 6 Paragraph 3).

One of ordinary skill in the art at the time the invention was made would combine the device of Goodrum and Cepulis with the routing table located in a ROM array of Microsoft, resulting in the invention of Claim 3, in order to provide a system which allows a PCI to PCI bridge add-in card in which the IRQ routing table only needs to describe the routing of the bridge's INTn# lines to the PCI interrupt router, or a transparent PCI to PCI bridge in which the IRQ routing table must report the IRQ routing for all devices behind the bridge, even when they are not present. Each of these devices provide a means for expanding the PCI bus in which a static routing table in a ROM array would be preferable to a dynamic routing table (See Page 6 Paragraph 7 and Page 7 Paragraphs 1-4 of Microsoft).

26. In reference to Claim 9, Goodrum and Cepulis teach the limitations as applied to Claim 8 above. Goodrum and Cepulis do not teach locating the routing table in a read-only memory in the computing device. Microsoft teaches locating the routing table in a ROM array (See Page 6 Paragraph 3).

One of ordinary skill in the art at the time the invention was made would combine the device of Goodrum and Cepulis with the routing table located in a ROM array of Microsoft, resulting in the invention of Claim 9, in order to provide a system which allows a PCI to PCI bridge add-in card in which the IRQ routing table only needs to describe the routing of the bridge's INTn# lines to the PCI interrupt router, or a transparent PCI to PCI bridge in which the IRQ routing table must report the IRQ routing for all devices behind the bridge, even when they are not present. Each of these devices provide a

means for expanding the PCI bus in which a static routing table in a ROM array would be preferable to a dynamic routing table (See Page 6 Paragraph 7 and Page 7 Paragraphs 1-4 of Microsoft).

27. In reference to Claim 15, Goodrum and Cepulis teach the limitations as applied to Claim 14 above. Goodrum and Cepulis do not teach locating the routing table in a read-only memory in the computing device. Microsoft teaches locating the routing table in a ROM array (See Page 6 Paragraph 3).

One of ordinary skill in the art at the time the invention was made would combine the device of Goodrum and Cepulis with the routing table located in a ROM array of Microsoft, resulting in the invention of Claim 15, in order to provide a system which allows a PCI to PCI bridge add-in card in which the IRQ routing table only needs to describe the routing of the bridge's INTn# lines to the PCI interrupt router, or a transparent PCI to PCI bridge in which the IRQ routing table must report the IRQ routing for all devices behind the bridge, even when they are not present. Each of these devices provide a means for expanding the PCI bus in which a static routing table in a ROM array would be preferable to a dynamic routing table (See Page 6 Paragraph 7 and Page 7 Paragraphs 1-4 of Microsoft).

28. Claims 19, 20, 21, 26, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goodrum and Cepulis.

29. In reference to Claim 19, Goodrum teaches a method executed internal to a computing device for identifying an available peripheral component interconnect (PCI) slot in the computing device, comprising: identifying a bus number and a device number for at least one PCI device coupled to a PCI bus coupled to the PCI slot (See Column 95 Lines 35-49); and identifying an unoccupied PCI slot (See Column 95 Lines 53-65). Goodrum does not teach locating a PCI IRQ routing table; identifying at least a bus number and a device number for each of a plurality of PCI slots using the routing table; comparing the bus number and the device number for each of the identified PCI slots to the bus number and the device number of at least one of the PCI devices; and based on the comparison of the bus number and the device number for at least one of the identified PCI slots and the bus number and the device number for at least one of the identified devices, determining if any of the identified PCI slots are unoccupied, an unoccupied PCI slot comprising an identified PCI slot that is not coupled to an identified PCI device. Cepulis teaches the use of a PCI Interrupt Request routing table to track PCI bus, device, and slot numbers for each PCI device slot (See Column 6 Lines 3-7); and comparing the PCI IRQ routing table Information for each PCI device slot (See Column 6 Lines 3-5) with the NVRAM data structure storing the information about each PCI device in the computer system (See Column 5 Lines 54-61) (See Column 6 Lines 26-28) and determining if any of the identified PCI slots are unoccupied based on the comparison of the bus number and the device number for at least one of the identified PCI slots and the bus number and the device number of the at least one of the identified devices (See Column 6 Lines 8-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Goodrum with the PCI IRQ routing table use and comparison of Cepulis, resulting in the invention of Claim 19, in order to provide a computing device that uses the most accurate copy of the bus, device, and slot numbers, since the table was loaded at startup and thus will reflect the most up to date configuration information of the system, as well as to allow configuration of the PCI devices at startup if their bus numbers have changed since the last time the information about each device was stored; as well as to allow configuration of the PCI devices at startup if their bus numbers have changed since the last time the information about each device was stored (See Column 6 Lines 11-25 of Cepulis).

30. In reference to Claim 20, Goodrum teaches a system for identifying an available peripheral component interconnect (PCI) slot in the computing device by executing an application internal to a computing device comprising: at least one computer readable medium (See Figure 1 Number 23 and Column 95 Lines 31-33); and software encoded on the at least one computer readable medium (See Column 95 Lines 26-33) and operable when executed by a processor to: identify a bus number and a device number for at least one PCI device coupled to a PCI bus coupled to the PCI slot (See Column 95 Lines 35-49); and identify an unoccupied PCI slot (See Column 95 Lines 53-65). Goodrum does not teach locating a PCI IRQ routing table; identifying at least a bus number and a device number for each of a plurality of PCI slots using the routing table; comparing the bus number and the device number for each of the identified PCI slots to

the bus number and the device number of at least one of the PCI devices; and based on the comparison of the bus number and the device number for at least one of the identified PCI slots and the bus number and the device number for at least one of the identified devices, determining if any of the identified PCI slots are unoccupied, an unoccupied PCI slot comprising an identified PCI slot that is not coupled to an identified PCI device. Cepulis teaches the use of a PCI Interrupt Request routing table to track PCI bus, device, and slot numbers for each PCI device slot (See Column 6 Lines 3-7); and comparing the PCI IRQ routing table Information for each PCI device slot (See Column 6 Lines 3-5) with the NVRAM data structure storing the information about each PCI device in the computer system (See Column 5 Lines 54-61) (See Column 6 Lines 26-28) and determining if any of the identified PCI slots are unoccupied based on the comparison of the bus number and the device number for at least one of the identified PCI slots and the bus number and the device number of the at least one of the identified devices (See Column 6 Lines 8-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Goodrum with the PCI IRQ routing table use and comparison of Cepulis, resulting in the invention of Claim 20, in order to provide a computing device that uses the most accurate copy of the bus, device, and slot numbers, since the table was loaded at startup and thus will reflect the most up to date configuration information of the system, as well as to allow configuration of the PCI devices at startup if their bus numbers have changed since the last time the information about each device was stored; as well as to allow configuration of the PCI devices at

startup if their bus numbers have changed since the last time the information about each device was stored (See Column 6 Lines 11-25 of Cepulis).

31. In reference to Claim 21, Goodrum teaches a system for identifying an available peripheral component interconnect (PCI) slot in the computing device by executing a process internal to a computing device, the system comprising: a memory (See Figure 1 Number 23 and Column 95 Lines 31-33); and a processor coupled to the memory (See Figure 1 Number 14) and operable to: identify a bus number and a device number for at least one PCI device coupled to a PCI bus coupled to the PCI slot (See Column 95 Lines 35-49); and identify an unoccupied PCI slot (See Column 95 Lines 53-65). Goodrum does not teach that the memory contains a PCI Interrupt Request routing table; locating the routing table in memory; identifying at least a bus number and a device number for each of a plurality of PCI slots using the routing table; comparing the bus number and the device number for each of the identified PCI slots to the bus number and the device number of at least one of the PCI devices; and based on the comparison of the bus number and the device number for at least one of the identified PCI slots and the bus number and the device number for at least one of the identified devices, determining if any of the identified PCI slots are unoccupied, an unoccupied PCI slot comprising an identified PCI slot that is not coupled to an identified PCI device. Cepulis teaches the use of a PCI Interrupt Request routing table to track PCI bus, device, and slot numbers for each PCI device slot (See Column 6 Lines 3-7); and comparing the PCI IRQ routing table Information for each PCI device slot (See Column

6 Lines 3-5) with the NVRAM data structure storing the information about each PCI device in the computer system (See Column 5 Lines 54-61) (See Column 6 Lines 26-28) and determining if any of the identified PCI slots are unoccupied based on the comparison of the bus number and the device number for at least one of the identified PCI slots and the bus number and the device number of the at least one of the identified devices (See Column 6 Lines 8-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Goodrum with the PCI IRQ routing table use and comparison of Cepulis, resulting in the invention of Claim 21, in order to provide a computing device that uses the most accurate copy of the bus, device, and slot numbers, since the table was loaded at startup and thus will reflect the most up to date configuration information of the system, as well as to allow configuration of the PCI devices at startup if their bus numbers have changed since the last time the information about each device was stored; as well as to allow configuration of the PCI devices at startup if their bus numbers have changed since the last time the information about each device was stored (See Column 6 Lines 11-25 of Cepulis).

32. In reference to Claim 26, Goodrum teaches a method executed internal to a computing device for identifying an available peripheral component interconnect (PCI) slot in the computing device, comprising: creating a table, which is equivalent to generating a list, of PCI slots associated with the computing device (See Column 95 Lines 16-25); and identifying, without requiring physical inspection of any PCI slots in

the computing device, an unoccupied PCI slot, an unoccupied PCI slot comprising an identified PCI slot that is not coupled to an identified PCI device (See Column 95 Lines 53-65). Goodrum does not teach generating a list of one or more PCI devices coupled to a PCI bus, the PCI bus coupled to the PCI slot; and identifying, without requiring physical inspection of any PCI slots in the computing device, an unoccupied PCI slot by comparing the list of PCI slots associated with the computing device with the list of one or more PCI devices coupled to the PCI bus. Cepulis teaches creating an NVRAM data structure that stores the information about each PCI device in the computer system, which is equivalent to generating a list of one or more PCI devices coupled to the PCI bus (See Column 5 Lines 54-61); and comparing the PCI IRQ routing table information for each PCI slot, which is equivalent to the list of PCI slots (See Column 6 Lines 3-5), with the NVRAM data structure storing the information about each PCI device in the computer system (See Column 5 Lines 54-61 and Column 6 Lines 26-28).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Goodrum with the NVRAM list and PCI IRQ routing table comparison of Cepulis, resulting in the invention of Claim 26, in order to provide a computing device that uses the most accurate copy of the bus, device, and slot numbers, since the table was loaded at startup and thus will reflect the most up to date configuration information of the system (See Column 6 Lines 11-25 of Cepulis) and to provide a means for storing the information regarding the presence of a device (See Column 5 Lines 38-42 of Cepulis) and to provide the information to the computer system faster upon startup (See Column 5 Lines 26-38 of Cepulis).

33. In reference to Claim 27, Goodrum teaches a method executed internal to a computing device for identifying an available peripheral component interconnect (PCI) slot in the computing device, comprising: generating an identification table identifying a plurality of PCI slots associated with the computing device (See Column 95 Lines 16-25); and identifying, without requiring physical inspection of any PCI slots in the computing device, an unoccupied PCI slot, an unoccupied PCI slot comprising an identified PCI slot that is not coupled to an identified PCI device (See Column 95 Lines 53-65). Goodrum does not teach generating an enumeration table enumerating one or more PCI devices coupled to a PCI bus, the PCI bus coupled to the PCI slot; and identifying, without requiring physical inspection of any PCI slots in the computing device, an unoccupied PCI slot by comparing the identification table and the enumeration table. Cepulis teaches creating an NVRAM data structure that stores the information about each PCI device in the computer system, which is equivalent an enumeration table, (See Column 5 Lines 54-61); and comparing the PCI IRQ routing table information for each PCI slot, which is equivalent to the identification table (See Column 6 Lines 3-5), with the NVRAM data structure storing the information about each PCI device in the computer system (See Column 5 Lines 54-61 and Column 6 Lines 26-28).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Goodrum with the NVRAM list and PCI IRQ routing table comparison of Cepulis, resulting in the invention of Claim 27, in order

to provide a computing device that uses the most accurate copy of the bus, device, and slot numbers, since the table was loaded at startup and thus will reflect the most up to date configuration information of the system (See Column 6 Lines 11-25 of Cepulis) and to provide a means for storing the information regarding the presence of a device (See Column 5 Lines 38-42 of Cepulis) and to provide the information to the computer system faster upon startup (See Column 5 Lines 26-38 of Cepulis).

Double Patenting

34. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

35. Claim 1 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 1 of U.S. Patent No. 6,772,252 in view of the Specification of U.S. Patent Number 6,772,252. Claim 1 of U.S. Patent Number 6,772,252 recites a method for identifying an available peripheral component

interconnect (PCI) slot in a computing device, comprising: identifying the one or more PCI slots in the computing device; identifying any PCI devices coupled to the PCI bus, the PCI bus coupled to the one or more PCI slots; and determining if any of the PCI slots are available without requiring physical inspection of the PCI slots, an available PCI slot comprising an identified PCI slot that is not coupled to an identified PCI bus. Claim 1 of U.S. Patent Number 6,772,252 differs from Claim 1 of the present application in that it fails to disclose that the method is executed internal to the computing system. However, the portion of the specification that supports Claim 1 of U.S. Patent Number 6,772,252 teaches that the method is performed internal to a computing device (See Figure 1 and Column 3 Line 66 – Column 6 Line 63), and thus it would be obvious to perform the method of Claim 1 internal to the computing device.

36. Claim 2 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 1 of U.S. Patent No. 6,772,252 in view of the Specification of U.S. Patent Number 6,772,252. Claim 2 recites all of the limitations of Claim 1, the double patenting rejection of which has been described above. Claim 1 of U.S. Patent Number 6,772,252 recites the further limitations of Claim 2 of the present application, namely identifying the one or more PCI slots in the computing device by identifying one or more bus numbers and one or more device numbers for the one or more PCI slots using a PCI Interrupt Request (IRQ) routing table.

37. Claim 4 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 2 of U.S. Patent No. 6,772,252 in view of the Specification of U.S. Patent Number 6,772,252. Claim 4 recites all of the limitations of Claim 1, the double patenting rejection of which has been described above. Claim 2 of U.S. Patent Number 6,772,252 recites the further limitations of Claim 4 of the present application, namely that identifying any PCI devices coupled to a PCI bus comprises identifying a bus number and a device number for each PCI device coupled to the PCI bus.

38. Claim 5 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 3 of U.S. Patent No. 6,772,252 in view of the Specification of U.S. Patent Number 6,772,252. Claim 5 recites all of the limitations of Claim 1, the double patenting rejection of which has been described above. Claim 3 of U.S. Patent Number 6,772,252 recites the further limitations of Claim 5 of the present application, namely that determining if any of the identified PCI slots are available comprises comparing a bus number and a device number of at least one of the identified PCI slots to a bus number and a device number of at least one of the identified PCI devices.

39. Claim 7 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 5 of U.S. Patent No. 6,772,252 in view of the Specification of U.S. Patent Number 6,772,252. Claim 5 of U.S. Patent

Number 6,772,252 recites a system for identifying an available peripheral component interconnect (PCI) slot in a computing device, comprising: at least one computer readable medium; and software encoded on the at least one computer readable medium and operable when executed by a processor to: identify the one or more PCI slots in the computing device; identify any PCI devices coupled to the PCI bus, the PCI bus coupled to the one or more PCI slots; and determine if any of the PCI slots are available without requiring physical inspection of the PCI slots, an available PCI slot comprising an identified PCI slot that is not coupled to an identified PCI bus. Claim 5 of U.S. Patent Number 6,772,252 differs from Claim 7 of the present application in that it fails to disclose that the method is executed internal to the computing system. However, the portion of the specification that supports Claim 5 of U.S. Patent Number 6,772,252 teaches that the method is performed internal to a computing device (See Figure 1 and Column 3 Line 66 – Column 6 Line 63), and thus it would be obvious to perform the method of Claim 7 internal to the computing device.

40. Claim 8 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 5 of U.S. Patent No. 6,772,252 in view of the Specification of U.S. Patent Number 6,772,252. Claim 8 recites all of the limitations of Claim 7, the double patenting rejection of which has been described above. Claim 5 of U.S. Patent Number 6,772,252 recites the further limitations of Claim 8 of the present application, namely identifying the one or more PCI slots in the computing device by identifying one or more bus numbers and one or more device

numbers for the one or more PCI slots using a PCI Interrupt Request (IRQ) routing table.

41. Claim 10 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 6 of U.S. Patent No. 6,772,252 in view of the Specification of U.S. Patent Number 6,772,252. Claim 10 recites all of the limitations of Claim 7, the double patenting rejection of which has been described above. Claim 6 of U.S. Patent Number 6,772,252 recites the further limitations of Claim 10 of the present application, namely that identifying any PCI devices coupled to a PCI bus comprises identifying a bus number and a device number for each PCI device coupled to the PCI bus.

42. Claim 11 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 7 of U.S. Patent No. 6,772,252 in view of the Specification of U.S. Patent Number 6,772,252. Claim 11 recites all of the limitations of Claim 7, the double patenting rejection of which has been described above. Claim 7 of U.S. Patent Number 6,772,252 recites the further limitations of Claim 11 of the present application, namely that the software is operable to determine if any of the identified PCI slots are available by comparing a bus number and a device number of at least one of the identified PCI slots to a bus number and a device number of at least one of the identified PCI devices.

43. Claim 13 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 9 of U.S. Patent No. 6,772,252 in view of the Specification of U.S. Patent Number 6,772,252. Claim 9 of U.S. Patent Number 6,772,252 recites a system for identifying an available peripheral component interconnect (PCI) slot in a computing device, comprising: a memory operable to store information identifying one or more types of interfaces in the computing device; a processor coupled to the memory and operable to: identify any PCI devices coupled to the PCI bus, the PCI bus coupled to the one or more PCI slots; and determine if any of the PCI slots are available without requiring physical inspection of the PCI slots, an available PCI slot comprising an identified PCI slot that is not coupled to an identified PCI bus. Claim 9 of U.S. Patent Number 6,772,252 differs from Claim 13 of the present application in that it fails to disclose that the method is executed internal to the computing system. However, the portion of the specification that supports Claim 9 of U.S. Patent Number 6,772,252 teaches that the method is performed internal to a computing device (See Figure 1 and Column 3 Line 66 – Column 6 Line 63), and thus it would be obvious to perform the method of Claim 9 internal to the computing device.

44. Claim 14 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 9 of U.S. Patent No. 6,772,252 in view of the Specification of U.S. Patent Number 6,772,252. Claim 14 recites all of the limitations of Claim 13, the double patenting rejection of which has been described above. Claim 9 of U.S. Patent Number 6,772,252 recites the further limitations of Claim

14 of the present application, namely identifying the one or more PCI slots in the computing device by identifying one or more bus numbers and one or more device numbers for the one or more PCI slots using a PCI Interrupt Request (IRQ) routing table.

45. Claim 16 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 10 of U.S. Patent No. 6,772,252 in view of the Specification of U.S. Patent Number 6,772,252. Claim 16 recites all of the limitations of Claim 13, the double patenting rejection of which has been described above. Claim 10 of U.S. Patent Number 6,772,252 recites the further limitations of Claim 16 of the present application, namely that the processor is operable to identify any PCI devices coupled to a PCI bus comprises identifying a bus number and a device number for each PCI device coupled to the PCI bus. Claim 10 of U.S. Patent Number 6,772,252 differs from Claim 16 of the present application in that it fails to disclose using a bus controller to identify any PCI devices coupled to a PCI bus. However, the portion of the specification that supports Claim 10 of U.S. Patent Number 6,772,252 teaches using a bus controller to identify any PCI devices coupled to a PCI bus (See Column 8 Lines 26-35), and thus it would be obvious to perform the method of Claim 10 using a bus controller.

46. Claim 17 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 11 of U.S. Patent No. 6,772,252 in

view of the Specification of U.S. Patent Number 6,772,252. Claim 17 recites all of the limitations of Claim 13, the double patenting rejection of which has been described above. Claim 11 of U.S. Patent Number 6,772,252 recites the further limitations of Claim 17 of the present application, namely that the processor is operable to determine if any of the identified PCI slots are available by comparing a bus number and a device number of at least one of the identified PCI slots to a bus number and a device number of at least one of the identified PCI devices.

47. Claim 19 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 13 of U.S. Patent No. 6,772,252 in view of the Specification of U.S. Patent Number 6,772,252. Claim 13 of U.S. Patent Number 6,772,252 recites a method for identifying an available peripheral component interconnect (PCI) slot in a computing device, comprising: locating a PCI Interrupt Request (IRQ) routing table; identifying a bus number and a device number for each PCI slot using the routing table; identifying a bus number and a device number for any PCI devices coupled to a PCI bus, the PCI bus coupled to the PCI slot; comparing the bus number and the device number of each one of the identified PCI slots to the bus number and the device number of at least one of the identified PCI devices; and based on the comparison, determining if any of the PCI slots are, an available PCI slot comprising an identified PCI slot that is not coupled to an identified PCI bus. Claim 13 of U.S. Patent Number 6,772,252 differs from Claim 19 of the present application in that it fails to disclose that the method is executed internal to the computing system.

However, the portion of the specification that supports Claim 13 of U.S. Patent Number 6,772,252 teaches that the method is performed internal to a computing device (See Figure 1 and Column 3 Line 66 – Column 6 Line 63), and thus it would be obvious to perform the method of Claim 13 internal to the computing device.

48. Claim 20 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 14 of U.S. Patent No. 6,772,252 in view of the Specification of U.S. Patent Number 6,772,252. Claim 14 of U.S. Patent Number 6,772,252 recites a system for identifying an available peripheral component interconnect (PCI) slot in a computing device, comprising: at least one computer readable medium; software encoded on the at least one computer readable medium and operable when executed by a processor to: locate a PCI Interrupt Request (IRQ) routing table; identify a bus number and a device number for each PCI slot using the routing table; identify a bus number and a device number for any PCI devices coupled to a PCI bus, the PCI bus coupled to the PCI slot; compare the bus number and the device number of each one of the identified PCI slots to the bus number and the device number of at least one of the identified PCI devices; and based on the comparison, determine if any of the PCI slots are, an available PCI slot comprising an identified PCI slot that is not coupled to an identified PCI bus. Claim 14 of U.S. Patent Number 6,772,252 differs from Claim 20 of the present application in that it fails to disclose that the method is executed internal to the computing system. However, the portion of the specification that supports Claim 14 of U.S. Patent Number 6,772,252 teaches that the

method is performed internal to a computing device (See Figure 1 and Column 3 Line 66 – Column 6 Line 63), and thus it would be obvious to perform the method of Claim 14 internal to the computing device.

49. Claim 21 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 15 of U.S. Patent No. 6,772,252 in view of the Specification of U.S. Patent Number 6,772,252. Claim 15 of U.S. Patent Number 6,772,252 recites a system for identifying an available peripheral component interconnect (PCI) slot in a computing device, comprising: a memory containing a PCI Interrupt Request (IRQ) routing table; and a processor operable to: locate the routing table; identify a bus number and a device number for each PCI slot using the routing table; identify a bus number and a device number for any PCI devices coupled to a PCI bus, the PCI bus coupled to the PCI slot; compare the bus number and the device number of each one of the identified PCI slots to the bus number and the device number of at least one of the identified PCI devices; and based on the comparison, determine if any of the PCI slots are, an available PCI slot comprising an identified PCI slot that is not coupled to an identified PCI bus. Claim 15 of U.S. Patent Number 6,772,252 differs from Claim 21 of the present application in that it fails to disclose that the method is executed internal to the computing system. However, the portion of the specification that supports Claim 15 of U.S. Patent Number 6,772,252 teaches that the method is performed internal to a computing device (See Figure 1 and Column 3 Line

66 – Column 6 Line 63), and thus it would be obvious to perform the method of Claim 21 internal to the computing device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The examiner can normally be reached on Monday-Thursday (7-4), Alt. Fridays (7-3).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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